

Phone : +91-40-2718 6619, 2718 2395 & 2718 2242, 2712 1013
 Fax : +91 -40-2712 1013 / 2712 3762
 E-mail : yhemalatha@ecil.co.in, rrc@ecil.co.in, cadmms@ecil.co.in



Electronics Corporation of India Limited

A Government of India Enterprise

CONTROL & AUTOMATION DIVISION-PURCHASE

ECIL Post, Hyderabad - 500 062.

ENQUIRY No. EC/PUR/TAD/

1964/929153

DATE: 2014.05.12

DUE DATE: 2014.06.02

Ph:

e-mail:

EXTRA COPY

Contact: Smt Y. HEMALATHA (SM)

Dear Sir(s),

Kindly submit you quotation in a Sealed Envelope Superscribing Enquiry No. and Due Date for the supply of the following items as per terms and conditions overleaf to PURCHASE MANAGER - CONTROL & AUTOMATION DIVISION ECIL, HYDERABAD-62. QUOTATIONS AGAINST EACH TENDER SHALL BE SENT IN SEPARATE ENVELOPE. QUOTATIONS RECEIVED AFTER THE DUE DATE AND TENDERS SENT IN OPEN/UNSUPERSCRIBED ENVELOPE WILL BE REJECTED. PLEASE SEND REGRET LETTER, IF YOU ARE NOT ABLE TO QUOTE TO CONTINUE TO KEEP YOUR NAME IN OUR MAILING LIST.

IMPORTANT INSTRUCTIONS

Parties must give the following information otherwise offer may be rejected.

- Unit Rate and Terms of price
- Quantity discount if any
- Rate of Excise Duty, Sales Tax if any
- Firm Delivery schedule
- Mode of despatch
- Estimated Packing and Forwarding Charges
- Validity of quotation
- Terms of payment
- Sales Tax Registration Number/
VAT and Service Tax Regn. No
- SSI/NSI Regn. No.

Sl.No.	Material Description and Specification	Estimated Requirement	
		Unit Code	Quantity
1	Supply, Installation and training of Synphony Model Compiler for Model based Design Entry and High Level synthesis to RTL from algorithmic description. Specification as per annexure 1 enclosed	Nos.	1
2	Synplify Premier for Synthesis (efficient conversion of HDL at RTL abstraction Level to gate level net-list). This software shall include HDL Analyst and Identity RTL Debugger. Specification as per annexure 1 enclosed Warranty: One year after completion installation and training. Note: You shall submit the authorization letter from OEM along with quotation. Terms and conditions as per annexure-2 enclosed.	Nos.	1

- NOTE:**
- CERTIFICATE OF COMPLIANCE/BATCH CERTIFICATE /CCQE/CMRI/ATX/WARRANTY TEST CERTIFICATE SHALL BE FURNISHED. PLEASE CONFIRM.
 - DATA SHEETS (CATALOGUES) SHALL BE SUPPLIED WITH THE QUOTATION.
 - IF THE MATERIAL IS COVERED UNDER DGS & D RATE CONTRACT. PLEASE QUOTE THE RATES ACCORDINGLY.
 - IF THE MATERIAL IS COVERED UNDER EXCISE, FURNISH EXCISE TARIFF NUMBER AND CLASSIFICATION.

Yours faithfully,

For Electronics Corporation of India Limited
 Y. HEMALATHA
 Purchase Manager
 सीएडी-ग्रुप / CAD-PURCHASE
 ई सी आई एल, हैदराबाद
 ECIL, HYDERABAD-500 062

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| 2. Quantity discount if any | 7. Validity of quotation |
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VAT and Service Tax Regn. No |
| 5. Mode of despatch | 10. SSI/NSI Regn. No. |

Sl.No.	Material Description and Specification	Estimated Requirement	
		Unit Code	Quantity
	<p><u>Special Notes.</u></p> <p>1. OUR PAYMENT TERMS ARE 30 DAYS CREDIT. PLEASE QUOTE WITH THE SAME TERMS.</p> <p>2. PLEASE SEND CATALOGUES AND DATA SHEETS ALONG WITH YOUR OFFER.</p> <p>3. PLEASE QUOTE TERMS OF PRICE AS FREE DELIVERY TO OUR STORES</p> <p>4. THE ABOVE MATERIALS ARE URGENTLY REQUIRED. PLEASE QUOTE EARLIEST DELIVERY DATE.</p> <p>5. IF YOU ARE UNABLE TO QUOTE, SEND REGRET LETTER POSITIVELY BY FAX/MAIL. OUR FAX NO 27121013 AND MAIL ID yhemalatha@ecil.co.in. TO ENABLE US TO KEEP YOU IN MAILING LIST.</p> <p>6. QUOTATIONS BY E-MAIL WILL NOT BE CONSIDERED. SEND HARD COPY ONLY.</p>		

- NOTE:**
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Yours faithfully,

For **Electronics Corporation of India Limited**

Y. HEMALATHA
 वरिष्ठ प्रबंधक / Senior Manager
 सीएडी - कंत्रा / CAD-PURCHASE
 ई सी आई एल, हैदराबाद
 ECIL, HYDERABAD-500 062

Annexure 1

Indent No: 929153

Project No: 64 – 245 – 24 – 000

1) Symphony Model Compiler, (Network Enabled Floating License)

It shall provide and support the following features:

- Automatic generation of synthesizable RTL from MATLAB code / Simulink models.
- Provide a vendor – independent solution for FPGA and ASIC implementation, with the generated RTL being fully synthesizable by latest release of any industry standard logic synthesis tool. However at the same time, the generated RTL should be optimized for the target device information provided by the user as part of the RTL generation process without printing any device specific macros.
- High-level synthesis optimization across multiple sample rates
- Automatic clock circuits generation and management of clocking strategies for multi-rate designs
- Automatic generation of synthesis design constraints with appropriate clock specification and appropriate multi-cycle path specifications for multi-rate designs
- Provide built-in up-samplers, down-samplers, FIFO and multi rate RAM primitives to easily design and model sample rate changes
- M-control for high-level specification of control logic using .m syntax.
- Easy To use primitives for building Mealy and Moore state machines
- Communications IP Library: contains blocks specific to the communications industry.
- Control logic IP Library: Contains blocks that implement logic for controlling data paths.
- DSP Library: Contains fundamental blocks for most DSP functions
- Filtering Library: Contains blocks for designing and implementing filters.
- Math Function Library: Contains blocks for specialized math operations.
- Floating Point Library: Contains several arithmetic blocks for direct floating point design on FPGA
- Transforms Library: Contains blocks for transforms that are important to DSP operations
- Automatic system- wide pipeline insertion and retiming to achieve target clock frequencies.
- Fixed point Analysis and debugging support
- IP –aware micro architecture optimization
- Automatic scheduling and time multiplexed resource shaping for area optimization
- Automated multi-channelization and resource sharing across channels.

Indt: 989153

- Target-aware optimization for FPGAs including automatic inferring of special resources like hardware multipliers, MACs, adders, memories and shift registers
- Ability to perform bottom up design using different optimization strategies for different parts of the design.
- High level reporting of number of processing elements (adder, multipliers, memory, registers etc) during RTL generation.
- User ability to control resource allocation: the tool should allow the user to specify at the Simulink level any resource constraints that is desired during implementation of the specific block / subsystem.
- User ability to control multi-cycle path specification from Simulink model
- Automatic generation of cycle accurate C model from Simulink design for faster system level simulation for functional verification
- Allow the user to import third party RTL into Simulink environment and the ability to integrate third RTL into the Simulink design as a Simulink block with automatic s-function generation for simulation
- Automatic generation of VHDL / Verilog testbench for the vectors applied in Simulink for simulation and scripts for RTL Simulation using VCS.
- Automatic derivation of switching activity from Simulink model for ASIC low power optimizations.
- Generate power optimized RTL
- Automatic generation of RTL constraints and scripts for Synplify Premier and DC for targeting ASICS.
- Advanced Timing estimation to generate RTL that is guaranteed to meet timing specification when Synplify Premier in loop

2) Synplify Premier (Node locked license)

It shall provide and support the following features:

- Automatically implements Triple Modular Redundancy (TMR) logic when enabled.
- Both logic synthesis and physical flows.
- Support synthesis from full behavioural RTL description, as well as a combination of WSYWIG device primitives and behavioural RTL.
- Compatible with both legacy parts as well as modern parts, e.g. for Xilinx support for all Virtex and Spartan families in all performance grades.
- Automatic conversion of large delays to RAMs.
- +Extract and infer RAMs (including non-zero initial states) and ROMs from behavioural RTL.
- Perform automatic inference of DSP blocks by looking for patterns across hierarchy.
- Ability to recognize multi-DSP patterns
- Automatic pipelining and register balancing to achieve higher clock speed.

Indt : 929153

- Support for user level synthesis programs to override default behaviours of RAM / DSP inference and cross hierarchical optimization.
- Optimized extraction and mapping of finite state machines.
- Seamless and one – click integration with vendor place and route tools.
- Automatic conversation of timing constraints to vendor specific formats.
- Automatic propagation of user constraints to PNR tool.
- Report all errors in single design iteration.
- Blackbox and graybox flows.
- Provides provision for integration of encrypted 3rd party IP.
- Constraint checking.
- Graphical RTL view and technology view as well as support for cross probing among them and with timing logs post synthesis and post PNR.
- Incremental synthesis.
- Automatic partitioning and parallel synthesis to speed up runtime without Quality of Result degradation.
- Safe and Fault Tolerant State Machine Design using Hamming -3 encoding.
- Automated documentation.
- Automatic RAM memory inference from the RTL.
- Built-in SynCore IP Generator for Automatic generation of technology-independent RTL for memories, FIFOs and arithmetic functions.
- Verilog, VHDL, System Verilog, VHDL-2008 and mixed –language designs.
- Built-in HDL Analyst for interactive debug, efficient constraints setting as well as cross-probing between RTL source code, netlist, RTL schematics, netlist schematics.
- Integrates seamlessly with Symphony Model Compiler.
- Built-in Real time debugging interface Identify which supports and provides for the following features:-
 - Ability to instrument and debug an advanced FPGA design directly from RTL source code.
 - Advanced trigger creation allows the viewing of desired design operation scenarios and probe specific nodes in the circuits.
 - Visibility into the internal design while operating at full speed.
 - Connects to live FPGA hardware using popular JTAG programming Interfaces
 - Selectively view up to 8 distinct groups of internal nodes with a single Identity IIICE during a debug session

Indent No: 929153

ANNEXURE-II

Commercial Terms and Conditions

1. Warranty shall be provided for a period of 12 months from the date of supply.
2. Performance Bank Guarantee (PBG) shall be provided for 10% value of the purchase Order during the warranty period.
3. Liquidated Damages: In the event of any delay in execution of the order beyond the Stipulated delivery schedule, ECIL, at their option, LD will be recovered @ 1/2% per week On the value of undelivered goods, subject to a maximum 5% of the total order value.
4. Risk Purchase Clause: In the event of any failure of the seller to comply with the Purchase order terms, the buyer has a right to cancel the order and proceed with an Vendor shall be liable to bear the extra cost which may incurred by the buyer.
5. Arbitration Clause: All disputes or differences whatever arising between two parties Out of relating construction meaning and operating of effect of this contract or the Breach of them shall be settled by arbitration in accordance with the rules of arbitration of The Indian Council of Arbitration is at Hyderabad/Secunderabad Jurisdiction.